**COURSE FILE**

**For**

**Digital Design (ECSE104L)**

Faculty Name : Vipul Kumar Mishra, Tanmay Bhowmik,

Akash Yadav

Course Type : Core

Semester and Year: 2nd Semester and 1st Year

L-T-P : 3-0-2

Credits : 4 credit

Department : Computer Science Engineering

Course Level : UG

**SCHOOL OF ENGINEERING AND APPLIED SCIENCES**

**Department of Computer Science Engineering**

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| Bennett University  Greater Noida, Uttar Pradesh |

**ECSE104L: Digital Design**

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| Course Type: | Core |  | L | T | P | Credits |
|  | | 3 | 0 | 2 | 4 |

Pre-requisites: NA

**Course Learning Outcomes:**

**CLO1:** Understand how analog signals are used to represent digital values in different logic families, including characterization of the noise margins.

**CLO2:** Create the appropriate truth table and gate level implementation from a description of a combinational logic function.

**CLO3:** Draw a circuit diagram for a sequential logic circuit and analyze its timing properties (input setup and hold times, minimum clock period, output propagation delays) and implement a substantial digital system on an FPGA.

**Module 1 (Contact hours: 12)**

Digital Systems; Data representation and coding; Logic circuits, integrated circuits; Analysis, design and implementation of digital systems; Introduction of CAD tools. Application of electric circuits, analog and digital electronics; Number system; Representation of signed numbers; Fixed and floating-point numbers; BCD; Gray codes; parity check codes and Hamming code; Definition and specification; Truth table; Basic logic operation and logic gates. Basic Boolean algebra; Standard representation and simplification of logic functions - K-map and tabular methods. Decoders, encoders, multiplexers, de multiplexers and their applications; Parity circuits and comparators.

**Module 2 (Contact hours: 12)**

Arithmetic modules-adders, CLA, multiplier, subtractors ALU Design examples. Definition of state machines, state machine as a sequential controller; Basic sequential circuits- latches and flip-flops: SR-latch, D-latch, Edge trigger and level trigger; D flip-flop, JK flip-flop, T flip-flop; Timing hazards and races; Analysis of state machines using D flip-flops and JK flip-flops; Multi-bit latches and registers, counters, shift register, application examples.

**Module 4 (Contact hours: 9)**

Design of state machines - state table, state assignment, transition/excitation table, excitation maps and equations, logic realization; Read-only memory, PROM, read/write memory - SRAM and DRAM PLAs, PALs and their applications; Sequential PLDs and their applications.

**Module 5 (Contact hours: 9)**

Designing state machine using ASM charts; Designing state machine using state diagram; Design examples State-machine design with sequential PLDs; Introduction to different logic families; TTL inverter - circuit description and operation; CMOS inverter - circuit description and operation; propagation delay, transition time, power consumption and power-delay product.

**Lab Experiments**

In this course students will start with basic digital components such as Arithmetic and logical operation, Memory etc. Then finally design soft IP.

**Suggested Textbooks:**

1. [*M. Morris Mano*](http://www.amazon.in/M.-Morris-Mano/e/B001ILKELA/ref=dp_byline_cont_book_1)*, Digital Design: with an Introduction to the Verilog HDL (5th Edition), Pearson, 2014.* ***ISBN-****978-9332535763*.

**References:**

1. *D. M. Harris and S. L. Harris, Digital Design and Computer Architecture (2nd Edition), Morgan Kaufmann, 2012. ISBN- 978-0123944245*.
2. *S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, (2nd Edition), Prentice Hall, 2003. ISBN- 978-0132599702*.

**Evaluation Components:**

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| **Components of Course Evaluation** | **Percentage** |
| Minor Examination | 20 |
| Assignment | 10 |
| Quiz | 15 |
| End-term Examination | 35 |
| Lab Evaluation | 20 |

**Lecture Wise Plan:**

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| **Lecture No.** | **Content Planned** |
| 1 | Introduction To Digital Circuits |
| 2 | Introduction To Digital Circuits |
| 3 | Number System |
| 4 | Combinational Logic Basics |
| 5 | Combinational Circuits |
| 6 | Logic Simplification |
| 7 | Karnaugh Maps And Implicants |
| 8 | Logic Minimization Using Karnaugh Maps |
| 9 | Karnaugh Map Minimization Using Maxterms |
| 10 | Code Converters |
| 11 | Parity Generators And Display Decoder |
| 12 | Arithmetic Circuits |
| 13 | Carry Look Ahead Adders |
| 14 | Subtractors |
| 15 | 2?'S Complement Subtractor and BCD Adder |
| 16 | Array Multiplier |
| 17 | Encoder Decoder |
| 18 | Mux Demux |
| 19 | Mux, DMux, Application |
| 20 | Buffer Lecture for revision |
| 21 | Introduction to Sequential Circuits |
| 22 | S-R, J-K and D Flip Flops |
| 23 | J-K and T Flip Flops |
| 24 | Triggering Mechanisms of Flip Flops and Counters |
| 25 | Up/ Down Counters |
| 26 | Shift Registers |
| 27 | Application of shift Registers |
| 28 | State Machines |
| 29 | Design of Synchronous Sequential Circuits |
| 30 | Design using J-K Flip Flop |
| 31 | Mealy and Moore Circuits |
| 32 | Pattern Detector |
| 33 | MSI and LSI Based Design |
| 34 | Multiplexer Based Design |
| 35 | Encoders and Decoders |
| 36 | Programmable Logic Devices |
| 37 | Design using Programmable Logic Devices |
| 38 | Design using Programmable Logic Devices (contd) |
| 39 | MSI and LSI based Implementation of Sequential Circuits |
| 40 | MSI and LSI based Implementation of Sequential Circuits (contd) |
| 41 | Design of circuits using MSI sequential blocks |
| 42 | Buffer Lecture for revision |

**Lab Plan**

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| **Lab No.** | **Content Planned** |
| 1 | Programming practice related to Number System conversion |
| 2 | Introduction to Verilog |
| 3 | Simplification of Boolean Function (Schematic Diagram + Verilog Code + Validation) |
| 4 | Implementation of Half Adder, 2’s complementor, Full Adder |
| 5 | Implementation of 4-bit Ripple Carry Adder, Implementation of 3:8 Decoder, Implementation of BCD to 7-Segment Decoder |
| 6 | Lab Evaluation 1 |
| 7 – 8 | Introduction to Latch, circuit + Hardware Implementation using FPGA |
| 9 – 10 | Introduction to Flipflop, circuit + Hardware Implementation using FPGA |
| 11 | Lab Evaluation 2 |
| 12 – 13 | Introduction to Counter, circuit + Hardware Implementation using FPGA |
| 14 | Lab Evaluation 3 |